REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-3, 5, 7, 9 and 11-17 are pending in the present application. By this Reply, claims 6 and 10 have been canceled, and claims 1, 7, 11 and 13 have been amended.

CLAIM REJECTIONS UNDER 35 USC § 103(a)

Claims 1-17 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Raghavan et al. in view of Strolle. This rejection is respectfully traversed.

Amended independent claim 1 includes a combination of elements and is directed to a Fixed-Delay Tree Search with Decision Feedback (FDTS/DF) equalizer including a feed-forward filter receiving and filtering a sampled signal, a feed-back filter filtering a restored data, a subtractor subtracting signals respectively filtered by the feed-forward filter and the feed-back filter, and a detector receiving the subtracted signal and detecting a data using an absolute value calculation. Further, the detector includes a plurality of branch metric calculating units obtaining an error between the subtracted signal and a reference signal, in which the reference signal is time-variant and is determined by the feed-back filter and by an original data detected by the detector, an adder adding the values outputted from the plurality of branch metric calculating units, a path metric memory storing the added value, a minimum value calculating unit calculating a minimum value of the accumulated values, and a comparator comparing the minimum values and outputting a most minimum value. Claim 1 has also been amended to clarify that the plurality of branch metric calculating units includes a plurality of absolute value

calculating units obtaining an absolute value of a difference between the subtracted signal and the reference signal, a demultiplexer demultiplexing the absolute value outputted from the plurality of absolute value calculating units, and an adding unit adding the demultiplexed value outputted from the demultiplexer and a path metric value prior to a one period of sampling time. Independent claims 7, 11 and 13 include similar features in varying scope.

These features are illustrated at least by the non-limiting example shown in Figure 4 and described at page 7, lines 17-24. For example, as shown in Figure 4, the plurality of branch metric calculating units (410) includes a plurality of absolute value calculating units (510) obtaining an absolute value of a difference between the subtracted signal Z_k and the reference signal Y_k, a demultiplexer (520) demultiplexing the absolute value obtained from the plurality of absolute value calculating units (510), and an adding unit (460) adding the demultiplexed value outputted from the demultiplexer (520) and a path metric value prior to a one period of sampling time. Thus, according to embodiments of the present invention, the number of gates may be reduced, a calculation speed may be improved, and the size of the chip may be reduced using the adding unit (460) in combination with the absolute value calculator (510) and demultiplexer (520). Fig. 6 illustrates the critical path of the present invention being less than for a mulitiplier.

Raghavan et al. discloses calculating an array of branch metrics for the input symbol, in which each branch metric in the array of branch metrics is a measure of the difference between the input symbol and an array of predicted input symbols. Raghavan et al. also discloses calculating a state metric for each of the A symbols in the symbol alphabet for the kth time step, the state metric being dependent on the state metric for the (k-1)th time step and the array of branch metrics, determining a comparison result for each of the A symbols in the symbol

alphabet in response to the state metric for each of the A symbols in the symbol alphabet and storing the comparison result for each of the A symbols for the kth time step in a traceback memory, and if the kth time step is a traceback time step, tracing back and outputting a best sequence of symbols based on the comparison results stored in the traceback memory.

However, Raghavan et al. does not teach or suggest at least the claimed plurality of absolute value calculating units as in the present invention.

Further, Strolle et al. discloses an input terminal 52, which is coupled to 1) a series connection of a first subtractor 302 and a first absolute value circuit 304, 2) a series connection of a second subtractor 306 and a second absolute value circuit 308, and 3) a third absolute value circuit 310. Further, the output terminal of the first absolute value circuit 304 produces a signal representing the branch metric BM3 and is coupled to a first input terminal of a first adder 312. An output terminal of the first adder is coupled to a first signal input terminal of a first multiplexer 314 and a first input terminal of a first comparator 316 (see col. 10, line 56 ~ col. 11, line 5 and Figure 4).

However, Strolle et al. also does not teach or suggest the claimed plurality of absolute value calculating units as in the present invention.

Accordingly, it is respectfully submitted independent claim 1, 7, 11 and 13 and each of the claims depending there from are allowable.

CONCLUSION

For the foregoing reasons and in view of the above clarifying amendments, the Examiner is respectfully requested to reconsider and withdraw all of the objections and rejections of record, and to provide an early issuance of a Notice of Allowance.

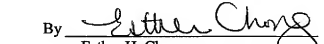
Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact David A. Bilodeau (Registration No. 42,325) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and further replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Date: January 23, 2008

Respectfully submitted,

BIRCH, STEWART, KOLASH & BIRCH, LLP

By 

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